Preliminary publication of JEDEC Semiconductor Memory Standard

This Standard was developed by JEDEC Committee JC-45 and approved by the JEDEC Board of Directors. It is published here in preliminary form, prior to being integrated into JESD21C, Release 14, and then published in final form.

Title of Standard: DDR2 SPD Revision 1.1

Council Ballot Number: JCB-04-005

Committee Ballot Numbers: 42.5-03-170, -230 -246, -247

Committee Item Numbers: 1489.02, 1542.01, 1468, 1502.03, 1489.03, 1392.03

Date of Council Approval: February 2004

Background: This proposal was balloted as JC-42.5-03-247 on November 11, 2003 and expired on December 3, 2003. The voting results were reported at the December 2003 JC-42 Committee meeting at which time the ballot was approved for Board of Directors submittal.

This BoD ballot contains the material of several committee ballots: Typically all these items would be scheduled to be included into a new SPD spec by Aug 2004, however in the December 2003 meeting a motion passed to include them asap. A TG was formed (chaired by DY Lee, Samsung) to incorporated all passed ballot regarding DDR2 SPD additions into a new DDR2 SPD specification revision: - DT in SPD #1468 --> BoD in 12/2003 - High temp SRF entry #1502.03 --> BoD in 12/2003 - Unique serial number #1489.03 --> ed change 9/2003 - Date encoding #1489.02 --> BoD in 9/2003 - Error/Typo in Byte 47 #1392.03 --> ed change 12/2003 - ADD/CMD Parity Byte 11 #1592.01 --> BoD in 12/2003 As one of the items includes a slight encoding changes (year/week encoding) the major revision number was due to be increased, however as this encoding change was fairly benign and there were concerns that existing BIOS would not be able to deal with a major revision increase in time, it was decided to call this new SPD revision 1.1. The TG also reviewed the revision 1.0 carefully and identified numerous inaccuracies and typos. These were corrected in this new Revision 1.1 as well

Appendix X: Specific PD's for DDR2 SDRAM (Revision 1.1)

1.0 Introduction

This appendix describes the presence detects for the DDR2 version of the synchronous DRAM modules. These PD's are those referenced in the SPD standard document for 'Specific Features'. The following SPD fields will occur in the order presented in section 1.1. Futher descriptions of Bytes 0 and 1 are found in the SPD standard. Further description of Byte 2 is found in Appendix A of the SPD standard. All unused entries wiil be coded as 00h. All unused bits in defined bytes will be coded as 0 except where noted.

1.1 Address map

The following is the SPD address map for DDR2 SDRAM. It describes where the individual LUT-entries will be held in the serial EEPROM.

Byte Number	Function Described	Notes
0	Number of Serial PD Bytes written during module production	1
1	Total number of Bytes in Serial PD device	2
2	Fundamental Memory Type (FPM, EDO, SDRAM, DDR, DDR2…)	
3	Number of Row Addresses on this assembly	
4	Number of Column Addresses on this assembly	
5	Number of DIMM Ranks	
6	Data Width of this assembly	
7	Reserved	
8	Voltage Interface Level of this assembly	
9	SDRAM Cycle time at Maximum Supported $\overline{\text{CAS}}$ Latency (CL), CL=X	3
10	SDRAM Access from Clock	
11	DIMM configuration type (Non-parity, Parity or ECC)	
12	Refresh Rate/Type	3, 4
13	Primary SDRAM Width	
14	Error Checking SDRAM Width	
15	Reserved	
16	SDRAM Device Attributes: Burst Lengths Supported	
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	3
18	SDRAM Device Attributes: $\overline{\text{CAS}}$ Latency	3
19	Reserved	3
20	DIMM Type Information	3
21	SDRAM Module Attributes	
22	SDRAM Device Attributes: General	3
23	Minimum Clock Cycle at CLX-1	3
24	Maximum Data Access Time (tAC) from Clock at CLX-1	3
25	Minimum Clock Cycle at CLX-2	3
26	Maximum Data Access Time (tAC) from Clock at CLX-2	3
27	Minimum Row Precharge Time (tRP)	3
28	Minimum Row Active to Row Active delay (tRRD)	3
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (tRCD)	3

Byte Number	Function Described	Notes
30	Minimum Active to Precharge Time (tRAS)	3
31	Module Rank Density	
32	Address and Command Input Setup Time Before Clock (tIS)	3
33	Address and Command Input Hold Time After Clock (tIH)	3
34	Data Input Setup Time Before Strobe (tDS)	3
35	Data Input Hold Time After Strobe (tDH)	3
36	Write recovery time (tWR)	3
37	Internal write to read command delay (tWTR)	3
38	Internal read to precharge command delay (tRTP)	3
39	Memory Analysis Probe Characteristics	
40	Extension of Byte 41 tRC and Byte 42 tRFC	
41	SDRAM Device Minimum Active to Active/Refresh Time (tRC)	3
42	SDRAM Device Minimum Refresh to Active/Refresh Command Period (tRFC)	3
43	SDRAM Device Maximum device cycle time (tCKmax)	3
44	SDRAM Device maximum skew between DQS and DQ signals (tDQSQ)	3
45	SDRAM Device Mazimum Read DataHold Skew Facktor (tQHS)	3
46	PLL Relock Time	
47	Bits 7:4: Tcasemax Delta (DRAM case temperature difference between maximum case temperature and baseline maximum case temperature), the baseline maximum case temperature is 85 degree C. Bits 3:0: DT4R4W Delta (Case temperature rise difference between IDD4R/ page open burst read and IDD4W/page open burst write operations).	7, 8, 11
48	Thermal resistance of DRAM device package from top (case) to ambient (Psi T-A DRAM) at still air condition based on JESD51-2 standard.	6, 10
49	DT0/Tcase Mode Bits: Bits 7:2:Case temperature rise from ambient due to IDD0/activate-precharge operation minus 2.8 degree C offset temperature. Bit 1: Double Refresh mode bit. Bit 0: High Temperature self-refresh rate support indication	7, 8, 11
50	DT2N/DT2Q: Case temperature rise from ambient due to IDD2N/precharge standby operation for UDIMM and due to IDD2Q/precharge quiet standby operation for RDIMM.	7, 8, 11
51	DT2P: Case temperature rise from ambient due to IDD2P/precharge power-down operation.	7, 8, 11
52	DT3N: Case temperature rise from ambient due to IDD3N/active standby operation.	7, 8, 11
53	DT3Pfast: Case temperature rise from ambient due to IDD3P Fast PDN Exit/active power-down with Fast PDN Exit operation.	7, 8, 11
54	DT3Pslow: Case temperature rise from ambient due to IDD3P Slow PDN Exit/active power-down with Slow PDN Exit operation.	7, 8, 11
55	DT4R/Mode Bit: Bits 7:1: Case temperature rise from ambient due to IDD4R/page open burst read operation. Bit 0: Mode bit to specify if DT4W is greater or less than DT4R.	7, 8, 11
56	DT5B: Case temperature rise from ambient due to IDD5B/burst refresh operation.	7, 8, 11
57	DT7: Case temperature rise from ambient due to IDD7/bank interleave read mode operation.	7, 8, 11
58	Thermal resistance of PLL device package from top (case) to ambient (Psi T-A PLL) at still air condition based on JESD51-2 standard.	6, 10
59	Thermal resistance of register device package from top (case) to ambient (Psi T-A Register) at still air condition based on JESD51-2 standard.	6, 10
60	DT PLL Active: Case temperature rise from ambient due to PLL in active mode at VCC = 1.9 volt, the PLL loading is the DIMM loading.	9, 11

Byte Number	Function Described	Notes
61	DT Register Active/Mode Bit: Bits 7:1: Case temperature rise from ambient due to register in active mode at VCC = 1.9 volt, the register loading is the RDIMM loading. Bit 0: mode bit to specify register data output toggle rate 50% or 100%.	9, 11
62	SPD Revision	
63	Checksum for Bytes 0-62	
64-71	Manufacturer's JEDEC ID Code	
72	Module Manufacturing Location	5
73-90	Module Part Number	5
91-92	Module Revision Code	5
93-94	Module Manufacturing Date	
95-98	Module Serial Number	
99-127	Manufacturer's Specific Data	5
128-255	Open for customer use	

1. This will typically be programmed as 128 Bytes.
2. This will typically be programmed as 256 Bytes.
3. From Datasheet.
4. High order bit is Self Refresh "flag". If set to "1", the assembly supports self refresh.
5. These are optional, in accordance with the JEDEC spec.
6. Refer to JESD51-3 "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages" under JESD51-2 standard.
7. DT parameter is derived as following: DTx = IDDx * VDD * Psi T-A, where IDDx definition is based on JEDEC DDR2 Component Specification and at VDD = 1.9 volt, it is the datasheet (worst case) value, and Psi T-A is the programmed value of Psi T-A (value in SPD Byte 48). Programmed temperature rise data (DTx) is based on the programmed value of Psi T-A (value in SPD byte 48).
8. All DT parameters are defined for DDR2 DRAM densities up to 2 Gbit. 4 Gbit parameters will be defined later.
9. DT parameters for PLL and register are derived as following: DTx = IDDx * VDD * Psi T-A, where IDDx definition is at VDD = 1.9 volt and it is the active PLL or register power corresponding to its respective DIMM configuration loading. The IDDx is the worst case value. Psi T-A used to program DTx is the programmed value of Psi T-A (value in SPD byte 58 or byte 59).
10. Rule for rounding off Psi T-A: Psi T-A shall be rounded such that it is nearest/closest to the true value of Psi T-A.
11. Rule for rounding off DTx: DTx shall be rounded such that it is nearest/closest to the calculated value of DTx.

2.0 Details of each byte

Byte 0: Number of Bytes Utilized by Module Manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Line #	Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 1: Total Number of Bytes in Serial PD Device

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor.

Line #	Serial Memory	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	2 Bytes	0	0	0	0	0	0	0	1	01
2	4 Bytes	0	0	0	0	0	0	1	0	02
3	8 Bytes	0	0	0	0	0	0	1	1	03
4	16 Bytes	0	0	0	0	0	1	0	0	04
5	32 Bytes	0	0	0	0	0	1	0	1	05
6	64 Bytes	0	0	0	0	0	1	1	0	06
7	128 Bytes	0	0	0	0	0	1	1	1	07
8	256 Bytes	0	0	0	0	1	0	0	0	08
9	512 Bytes	0	0	0	0	1	0	0	1	09
10	1024 Bytes	0	0	0	0	1	0	1	0	0A
11	2048 Bytes	0	0	0	0	1	0	1	1	0B
12	4096 Bytes	0	0	0	0	1	1	0	0	0C
13	8192 Bytes	0	0	0	0	1	1	0	1	0D
14	16384 Bytes	0	0	0	0	1	1	1	0	0E
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	-	1	1	1	1	1	1	1	0	FE
255	-	1	1	1	1	1	1	1	1	FF

Byte 2: Memory Type

This byte describes the fundamental memory type (or technology) implemented on the module.

Line #	Fundamental Memory Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Reserved	0	0	0	0	0	0	0	0	00
1	Standard FPM DRAM	0	0	0	0	0	0	0	1	01
2	EDO	0	0	0	0	0	0	1	0	02
3	Pipelined Nibble	0	0	0	0	0	0	1	1	03
4	SDRAM	0	0	0	0	0	1	0	0	04
5	ROM	0	0	0	0	0	1	0	1	05
6	SGRAM DDR	0	0	0	0	0	1	1	0	06
7	SDRAM DDR	0	0	0	0	0	1	1	1	07
8	DDR2 SDRAM	0	0	0	0	1	0	0	0	08
-	-	-	-	-	-	-	-	-	-	-
253	TBD	1	1	1	1	1	1	0	1	FD
254	TBD	1	1	1	1	1	1	1	0	FE
255	TBD	1	1	1	1	1	1	1	1	FF

Byte 3: Number of Row Addresses

This field describes the Row addressing on the module. bit 0-3 are used to represent the number of row addresses, bit 4-7 are reserved and should be coded as ‘0’

Examples of Byte 3 implementation include:

Number of Row Addresses	Module Organization	Device Used	Byte 3 Contents
13, RA0-RA12	32M x 64	32M x 16	0000 1101
14, RA0-RA13	64M x 64	64M x 8	0000 1110

Line #	Number of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 4: Number of Column Addresses

This field describes the Column addressing on the module. bit 0-3 are used to represent the number of column addresses, bit 4-7 are reserved and should be coded as '0'

For example:

Number of Column Addresses	Module Organization	Device Used	Byte 4 Contents
10, CA0-CA9	32M x 64	32M x 16	0000 1010
10, CA0-CA9	64M x 64	64M x 8	0000 1010

Line #	Number of Column Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 5: Module Attributes - Number of Ranks, Package and Height

This field describes the number of ranks (Rank: any DRAMs connected to same physical $\overline{CS}$) and package on the SDRAM module, and module height. The number of logical banks for the SDRAM device is defined in Byte 17.

Bit 7 ~ Bit 5	Bit 4	Bit 3	Bit 2 ~ Bit 0
Module Height	DRAM Packgage	Card on Card	# of Ranks
Bit[7, 6, 5] 000 = less than 25.4 mm 001 = 25.4 mm 010 = greater than 25.4 mm and less than 30 mm 011 = 30.0 mm 100 = 30.5 mm 101 = greater than 30.5 mm others :reserved	1 = stack 0 = planar	1 = yes 0 = no	Bit [2, 1, 0] : 000 = 1 rank 001 = 2 ranks 010 = 3 ranks 011 = 4 ranks ..... 111 = 8 ranks

Byte 6: Module Data Width

Byte 6 is used to designate the module's data width. For example:

Line #	Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not defined	0	0	0	0	0	0	0	0	0	00
-	-	-	-	-	-	-	-	-	-	-
32	32	0	0	1	0	0	0	0	0	20
33	33	0	0	1	0	0	0	0	1	21
-	-	-	-	-	-	-	-	-	-	-
36	36	0	0	1	0	0	1	0	0	24
-	-	-	-	-	-	-	-	-	-	-
64	64	0	1	0	0	0	0	0	0	40
-	-	-	-	-	-	-	-	-	-	-
72	72	0	1	0	0	1	0	0	0	48
-	-	-	-	-	-	-	-	-	-	-
80	80	0	1	0	1	0	0	0	0	50
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
144	144	1	0	0	1	0	0	0	0	90
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 7: Reserved

Byte 8: Voltage Interface Level of this assembly

This field describes the module's voltage interface.

Line #	Interface Levels	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	TTL/5V tolerant	0	0	0	0	0	0	0	0	00
1	LVTTL (not 5V tolerant)	0	0	0	0	0	0	0	1	01
2	HSTL 1.5V	0	0	0	0	0	0	1	0	02
3	SSTL 3.3V	0	0	0	0	0	0	1	1	03
4	SSTL 2.5V	0	0	0	0	0	1	0	0	04
5	SSTL 1.8V	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-

Byte 9: SDRAM Cycle Time

This byte defines the minimum cycle time for the SDRAM module at the highest $\overline{\text{CAS}}$ Latency, $\overline{\text{CAS}}$ Latency =X, defined in byte 18. If other $\overline{\text{CAS}}$ latencies are supported, then the associated minimum cycle times are not related in this version of the SPD standard. Byte 9, Cycle time for CAS Latency=X, is split into two nibbles: the higher order nibble (bits 4-7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of .1ns and is added to the value designated by the higher nibble. In addition, four lines of the lower order nibble are assigned to support +.25,+.33, +.66 and +.75. For example:

If bits 7:4 are	and bits 3:0 are	then the total time is:
0011	1101	
(3ns)	+ (.75ns)	= 3.75ns

Byte 9, SDRAM Cycle Time, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	**Cycle Time**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0					0_
1A	1ns	0	0	0	1					1_
2A	2ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1	See Subfield Table B				7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1					F_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 9, SDRAM Cycle Time Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	**Cycle Time**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0B	+0ns					0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	+.25ns					1	0	1	0	_A
11B	+.33ns					1	0	1	1	_B
12B	+.66ns					1	1	0	0	_C
13B	+.75ns					1	1	0	1	_D
-	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

See Subfield Table B

Byte 10: SDRAM Access from Clock (t_{AC})

This byte defines the maximum clock to data out for the SDRAM module. This is the Clock to data out specification at the highest given CAS Latency specified in byte 18 of this SPD specification. If other CAS latencies are supported, then the associated Maximum Clock Access times are not related in this version of the SPD standard. The byte is split into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0011	0101	
(0.3ns)	+ (0.05ns)	= 0.35ns

Byte 10: SDRAM Access from Clock, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0					0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1	See Subfield B				5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 10: SDRAM Access from Clock Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns					0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns			See Subfield A		0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 11: DIMM Configuration Type

This byte describes the module's error detection and/or correction schemes on the data, address and command buses.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	TBD	Address/Command Parity	Data ECC	Data Parity
0	0	0	0	0	1 or 0	1 or 0	1 or 0

1 = Supported on this assembly, 0 = Not supported on this assembly.
Note: Data ECC includes Data Parity, therefore modules with Data ECC shall encode bit 1 as 1 and bit 0 as 0.

Byte 12: Refresh Rate/Type

This byte describes the module's refresh rate.

Line #	Refresh Period	Bit 7 (Self Refresh Flag)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Normal (15.625 us)	0	0	0	0	0	0	0	0	00
1	Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1	01
2	Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0	02
3	Extended (2x)...31.3us	0	0	0	0	0	0	1	1	03
4	Extended (4x)...62.5us	0	0	0	0	0	1	0	0	04
5	Extended (8x)...125us	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
7	TBD	0	0	0	0	0	1	1	1	07
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-

Byte 13: Primary SDRAM Width

Bits 0-7 of this byte indicate the width of the primary data SDRAM. The primary SDRAM is that which is used for data; examples of primary (data) SDRAM widths are x4, x8, x16, and x32. Note that if the module is made with SDRAMs which provide for data and error checking, e.g. x9, x18, and x36, then it is also designated in this field.

This table contains examples of SDRAM DIMM

Module Width	Primary SDRAM Width	Error Checking SDRAM Width	Byte 13 Contents
x72	x8	x8	0000 1000
x72	x16	x16	0001 0000

Line #	SDRAM Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 14: Error Checking SDRAM Width

If the module incorporates error checking and if the primary data SDRAM does not include these bits — i.e. there are separate error checking SDRAMs — then the error checking SDRAM's width is expressed in this byte. Bits 0-7 of this byte relate the error checking SDRAM's width.

The following table contains examples of error checking SDRAM widths

Module Width	Primary SDRAM Width	Error Checking SDRAM Width	Possible (512Mb based) Module Density	Byte 14 Contents
x72	x8	x8	512 MB	0000 1000
x72	x16	x16	256 MB	0001 0000

Line #	Error Checking SDRAM Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 15: Reserved

Byte 16: SDRAM Device Attributes – Burst Lengths Supported

This byte describes which various programmable burst lengths are supported by the devices on the module. If the bit is “1”, then that Burst Length is supported on the module; if the bit is “0”, then that Burst Length is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	TBD	TBD
0	0	0	0	1 or 0	1 or 0	0	0
1 = Supported on this assembly, 0 = Not supported on this assembly.							

Byte 17: SDRAM Device Attributes – Number of Banks on SDRAM Device

This byte details how many banks are on each SDRAM installed onto the module.

Line #	Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
4	4	0	0	0	0	0	1	0	0	04
-	-	-	-	-	-	-	-	-	-	-
8	8	0	0	0	0	1	0	0	0	08
-	-	-	-	-	-	-	-	-	-	-
255	255	1	1	1	1	1	1	1	1	FF

Byte 18: SDRAM Device Attributes – $\overline{\text{CAS}}$ Latency

This byte describes which of the programmable $\overline{\text{CAS}}$ latencies are acceptable for the module. If the bit is “1”, then that $\overline{\text{CAS}}$ latency is supported on the module; if the bit is “0”, then that $\overline{\text{CAS}}$ latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	$\overline{\text{CAS}}$ Latency = 5	$\overline{\text{CAS}}$ Latency = 4	$\overline{\text{CAS}}$ Latency = 3	$\overline{\text{CAS}}$ Latency = 2	TBD	TBD
0	0	1 or 0	1 or 0	1 or 0	1 or 0	0	0
1 = Supported on this assembly; 0 = Not supported on this assembly.							

Byte 19: Reserved

Byte 20: DIMM type information

This byte describes the DIMM type information of DDR2 SDRAM.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	Mini-UDIMM (82.0 mm)*	Mini-RDIMM (82.0 mm)*	Micro-DIMM (45.5 mm)*	SO-DIMM (67.6 mm)*	Regular UDIMM (133.35 mm)*	Regular RDIMM (133.35 mm)*
0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

1 = Supported on this assembly; 0 = Not supported on this assembly.
* numbers shown are module width

Byte 21: SDRAM Modules Attributes

This byte depicts various aspects of the module. It details various unrelated but critical elements pertinent to the module. A given module characteristic is detailed in the designated bit. Bit 1:0 defines the number of active registers on the DIMM, the active register is defined as being in active mode with clock running within spec and OE enabled. If two registers do not have a common select S inputs, only one is considered active. Bit 3:2 defines the number of PLLs on the DIMM. Please refer to Byte 20 for DIMM type information.

Bit 7	Bit 6	Bit 5	Bit 4	Bit [3:2]	Bit [1:0]
TBD	Analysis probe installed*	TBD	FET Switch External Enable	Number of PLLs on the DIMM	Number of Active Registers on the DIMM**
0	1 or 0	0	1 or 0	00 : 0 01 : 1 10 : 2 11 : Reserved for future use	00 : 1 01 : 2 10 : 3 11 : 4

1 = Included on this assembly; 0 = Not included on this assembly.
* All normal DIMMs will set bit 6 to 0. If bit 6 is set to a 1 this indicates that a memory bus analysis probe is installed in the slot. The BIOS should ensure that Address and Command bus clocks remain turned for that slot and byte 39 may be optionally consulted to determine probe characteristics
** Bits 1:0 are only applicable if Byte 20 [Bit0 or Bit4] are set to 1. If Byte 20 [Bit0 and Bit4] are both set to 0, then Byte 21 Bit[1:0] are "don't care", and recommended content in this case is "00".

Byte 22: SDRAM Device Attributes – General

This byte depicts various aspects of the SDRAMs on the module. It details various unrelated but critical elements pertinent to the SDRAMs. A given SDRAM characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is "1". Conversely, if the aspect is FALSE, the designated bit is "0".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	TBD	TBD	TBD	Supports Weak Driver
0	0	0	0	0	0	0	1 or 0

Byte 23: Minimum Clock Cycle Time at Reduced $\overline{\text{CAS}}$ Latency, X- 1

The highest $\overline{\text{CAS}}$ latency identified in byte 18 is X and the timing values associated with $\overline{\text{CAS}}$ latency 'X' are found at byte locations 9 and 10. Byte 23 denotes the minimum cycle time at $\overline{\text{CAS}}$ latency X- 1.

For example, if byte 18 denotes $\overline{\text{CAS}}$ latencies of 3 to 4, then X is 4 and X-1 is 3. Byte 23 then denotes the minimum cycle time at $\overline{\text{CAS}}$ latency 3.

Byte 23 is split into two nibbles: the higher order nibble (bits 4-7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of .1ns and is added to the value designated by the higher nibble. In addition, four lines of the lower order nibble are assigned to support +0.25,+.33, +.66 and +.75. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is
0011	1011	
(3ns)	+ (.75ns)	=3.75ns

Byte 23, SDRAM Minimum Cycle Time @ CL X-1, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0					0_
1A	1ns/16ns	0	0	0	1					1_
2A	2ns/17ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1		See Subfield B			7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1					F_

Byte 23, SDRAM Minimum Cycle Time @ CL X-1, Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns					0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns			See Subfield A		0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	+.25ns					1	0	1	0	_A
11B	+.33ns					1	0	1	1	_B
12B	+.66ns					1	1	0	0	_C
13B	+.75ns					1	1	0	1	_D
-	.	.	.	.	.	.	.	.	.	.
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 24: Maximum Data Access Time (t_{AC}) from Clock at CL X- 1

The highest $\overline{CAS}$ latency identified in byte 18 is X. Byte 23 denotes the maximum access time from Clock at $\overline{CAS}$ latency X- 1.

For example, if byte 18 denotes supported $\overline{CAS}$ latencies of 3 to 4, then X is 4 and X-1 is 3. Byte 24 then denotes the maximum clock access time from CK at $\overline{CAS}$ latency 3.

Byte 24 is split into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0011	0101	
(0.3 ns)	+ (0.05 ns)	= 0.35 ns

Byte 24: SDRAM Access from Clock @ X-1, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0					0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1	See Subfield B				5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 24: SDRAM Access from Clock @ X-1, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns					0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns			See Subfield A		0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 25: Minimum Clock Cycle Time at CL X-2

The highest $\overline{\text{CAS}}$ latency identified in byte 18 is X. Byte 25 denotes the minimum cycle time at $\overline{\text{CAS}}$ latency X-2.

For example, if byte 18 denotes $\overline{\text{CAS}}$ latencies of 3 to 5, then X is 5 and X-2 is 3. Byte 25 then denotes the minimum cycle time at $\overline{\text{CAS}}$ latency 3.

Byte 25 is split into two nibbles: the higher order nibble (bits 4-7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of .1ns and is added to the value designated by the higher order nibble. In addition, four lines of the lower order nibble are assigned to support +0.25,+.33, +.66 and +.75. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
0011	1011	
(3 ns)	+ (.75 ns)	= 3.75 ns

Byte 25, SDRAM Minimum Cycle Time @ CL X-2, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	1ns/16ns	0	0	0	1					1_
2A	2ns/17ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1					F_

Byte 25, SDRAM Minimum Cycle Time @ CL X-2, Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	+.25ns					1	0	1	0	_A
11B	+.33ns					1	0	1	1	_B
12B	+.66ns					1	1	0	0	_C
13B	+.75ns					1	1	0	1	_D
-	.	.	.	.	.	.	.	.	.	.
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 26: Maximum Data Access Time (t_{AC}) from Clock at CL X-2

The highest $\overline{CAS}$ latency identified in byte 18 is X. Byte 26 denotes the maximum access time from Clock at $\overline{CAS}$ latency X-2.

For example, if byte 18 denotes supported $\overline{CAS}$ latencies of 3 to 5, then X is 5 and X-2 is 3. Byte 26 then denotes the maximum data access time from CK at $\overline{CAS}$ latency 3.

Byte 26 is split into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0011	0101	
(0.3ns)	+ (0.05ns)	= 0.35ns

Byte 26: SDRAM Access from Clock @ CL = X-2, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0					0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1		See Subfield B			5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 26: SDRAM Access from Clock @ CL = X-2, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns					0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns					0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 27: Minimum Row Precharge Time (t_{RP})

Byte 27 is used to designate the module's minimum Row Precharge time.

Byte 27 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001111 (15ns)	00 +(0.0ns)	= 15.0ns
010010 (18ns)	11 +(.75ns)	= 18.75ns

Byte 27, SDRAM Minimum t_{RP} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 27, SDRAM Minimum t_{RP} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1

Byte 28: Minimum Row Active to Row Active Delay (t_{RRD})

This field describes the minimum required delay between different row activations.

Byte 28 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
000111 (7ns)	10 +(0.5ns)	= 7.5ns
001010 (10ns)	00 +(0.0ns)	= 10ns

Byte 28, SDRAM Minimum t_{RRD} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 28, SDRAM Minimum t_{RRD} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1

Byte 29: Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD})

This byte describes the minimum delay required between assertions of $\overline{RAS}$ and $\overline{CAS}$ to the same bank.

Byte 29 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001111 (15ns)	00 +(0.0ns)	= 15.0ns
010010 (18ns)	11 +(.75ns)	= 18.75ns

Byte 29, SDRAM Minimum t_{RCD} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 29, SDRAM Minimum t_{RCD} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1

Byte 30: Minimum Active to Precharge Time (t_{RAS})

This byte identifies the minimum active to precharge time.

Minimum Active to Precharge Time (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF

Byte 31: Module Rank Density

This byte describes the density of each physical rank on the SDRAM DIMM. This byte will have only one bit set to “1” to represent per rank density. If there are more than one physical rank on the module (as represented in byte 5), then total density can be calculated by multiplying rank density in this field by number ranks described in byte 5.

For example:

Density of Physical Rank	Byte 31 Contents
512MB	1000 0000
256MB	0100 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
512 MB	256 MB	128 MB	16 GB	8 GB	4 GB	2 GB	1 GB
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
1 = Supported on this assembly; 0 = Not supported on this assembly.							

Byte 32: Address and Command Setup Time Before Clock (tIS)

This field describes the input setup time before the rising edge of the clock. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. Spec numbers that are in fractions of 0.01 ns will be rounded down (e.g. if the spec number is 375 ps, then 0.37 [ns] will be programmed in this field). Setup and hold time numbers are to be interpreted exactly as they are defined in JESD79-2 (Release 2).

For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
1011 (1.1ns)	0000 + (0ns)	= 1.1ns
1100 (1.2ns)	0101 + (0.05ns)	= 1.25ns

Byte 32: SDRAM Setup Time Before Clock, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1					5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	1.0ns	1	0	1	0					A_
11A	1.1ns	1	0	1	1					B_
12A	1.2ns	1	1	0	0					C_
13A	RFU	1	1	0	1					D_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 32: SDRAM Setup Time Before Clock, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns					0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 33: Address and Command Hold Time After Clock (tIH)

This field describes the input hold time after the rising edge of the clock. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. Spec numbers that are in fractions of 0.01 ns will be rounded down (e.g. if the spec number is 375 ps, then 0.37 [ns] will be programmed in this field). Setup and hold time numbers are to be interpreted exactly as they are defined in JESD79-2 (Release 2).

For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
1011 (1.1 ns)	0000 + (0 ns)	= 1.1 ns
1100 (1.2 ns)	0101 + (0.05 ns)	= 1.25 ns

Byte 33: SDRAM Hold Time After Clock, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0					0_
1A	.1 ns	0	0	0	1					1_
2A	.2 ns	0	0	1	0					2_
3A	.3 ns	0	0	1	1					3_
4A	.4 ns	0	1	0	0					4_
5A	.5 ns	0	1	0	1		See Subfield B			5_
6A	.6 ns	0	1	1	0					6_
7A	.7 ns	0	1	1	1					7_
8A	.8 ns	1	0	0	0					8_
9A	.9 ns	1	0	0	1					9_
10A	1.0 ns	1	0	1	0					A_
11A	1.1 ns	1	0	1	1					B_
12A	1.2 ns	1	1	0	0					C_
13A	RFU	1	1	0	1					D_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 33: SDRAM Hold Time After Clock, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0 ns					0	0	0	0	_0
1B	+.01 ns					0	0	0	1	_1
2B	+.02 ns					0	0	1	0	_2
3B	+.03 ns					0	0	1	1	_3
4B	+.04 ns					0	1	0	0	_4
5B	+.05 ns		See Subfield A			0	1	0	1	_5
6B	+.06 ns					0	1	1	0	_6
7B	+.07 ns					0	1	1	1	_7
8B	+.08 ns					1	0	0	0	_8
9B	+.09 ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 34: Data Input Setup Time Before Strobe (tDS)

This field describes the input setup time before the rising edge of the strobe. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designates the time to a granularity of 0.1 ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01 ns and is added to the value designated by the higher nibble. Spec numbers that are in fractions of 0.01 ns will be rounded down (e.g. if the spec number is 375 ps, then 0.37 [ns] will be programmed in this field). Setup and hold time numbers are to be interpreted exactly as they are defined in JESD79-2 (Release 2).

For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0010	0101	
(0.2 ns)	+(0.05 ns)	= 0.25 ns

Byte 34: SDRAM Setup Time Before Strobe, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0					0_
1A	.1 ns	0	0	0	1					1_
2A	.2 ns	0	0	1	0					2_
3A	.3 ns	0	0	1	1					3_
4A	.4 ns	0	1	0	0					4_
5A	.5 ns	0	1	0	1		See Subfield B			5_
6A	.6 ns	0	1	1	0					6_
7A	.7 ns	0	1	1	1					7_
8A	.8 ns	1	0	0	0					8_
9A	.9 ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 34: SDRAM Setup Time Before Strobe, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0 ns					0	0	0	0	_0
1B	+.01 ns					0	0	0	1	_1
2B	+.02 ns					0	0	1	0	_2
3B	+.03 ns					0	0	1	1	_3
4B	+.04 ns					0	1	0	0	_4
5B	+.05 ns		See Subfield A			0	1	0	1	_5
6B	+.06 ns					0	1	1	0	_6
7B	+.07 ns					0	1	1	1	_7
8B	+.08 ns					1	0	0	0	_8
9B	+.09 ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 35: Data Input Hold Time After Strobe (tDH)

This field describes the input hold time after the rising edge of the strobe. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designate the time to a granularity of 0.1 ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. Spec numbers that are in fractions of 0.01 ns will be rounded down (e.g. if the spec number is 375 ps, then 0.37 [ns] will be programmed in this field). Setup and hold time numbers are to be interpreted exactly as they are defined in JESD79-2 (Release 2).

For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0010	0101	
(0.2 ns)	+ (0.05 ns)	= 0.25 ns

Byte 35: SDRAM Hold Time After Strobe, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0					0_
1A	.1 ns	0	0	0	1					1_
2A	.2 ns	0	0	1	0					2_
3A	.3 ns	0	0	1	1					3_
4A	.4 ns	0	1	0	0					4_
5A	.5 ns	0	1	0	1		See Subfield B			5_
6A	.6 ns	0	1	1	0					6_
7A	.7 ns	0	1	1	1					7_
8A	.8 ns	1	0	0	0					8_
9A	.9 ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 35: SDRAM Hold Time After Strobe, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0 ns					0	0	0	0	_0
1B	+.01 ns					0	0	0	1	_1
2B	+.02 ns					0	0	1	0	_2
3B	+.03 ns					0	0	1	1	_3
4B	+.04 ns					0	1	0	0	_4
5B	+.05 ns					0	1	0	1	_5
6B	+.06 ns					0	1	1	0	_6
7B	+.07 ns					0	1	1	1	_7
8B	+.08 ns					1	0	0	0	_8
9B	+.09 ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 36: Write Recovery Time (t_{WR})

This byte describes the write recovery time(t_{WR})

Byte 36 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1 ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25 ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001111 (15 ns)	00 +(0.0 ns)	= 15.0 ns
010010 (18 ns)	11 +(.75 ns)	= 18.75 ns

Byte 36, SDRAM Minimum t_{WR} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1 ns	0	0	0	0	0	1		
2 ns	0	0	0	0	1	0		
3 ns	0	0	0	0	1	1		
4 ns	0	0	0	1	0	0		
5 ns	0	0	0	1	0	1		
6 ns	0	0	0	1	1	0		
7 ns	0	0	0	1	1	1		
8 ns	0	0	1	0	0	0		
9 ns	0	0	1	0	0	1		
10 ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61 ns	1	1	1	1	0	1		
62 ns	1	1	1	1	1	0		
63 ns	1	1	1	1	1	1		

Byte 36, SDRAM Minimum t_{WR} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0 ns	See Subfield A						0	0
+.25 ns							0	1
+.50 ns							1	0
+.75 ns							1	1

Byte 37: Internal write to read command delay (t_{WTR})

This byte describes the internal write to read command delay(t_{WTR})

Byte 37 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1 ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001010 (10 ns)	00 +(0.0 ns)	= 10.0 ns
000111 (7 ns)	10 +(.50 ns)	= 7.5 ns

Byte 37, SDRAM Minimum t_{WTR} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1 ns	0	0	0	0	0	1		
2 ns	0	0	0	0	1	0		
3 ns	0	0	0	0	1	1		
4 ns	0	0	0	1	0	0		
5 ns	0	0	0	1	0	1		
6 ns	0	0	0	1	1	0		
7 ns	0	0	0	1	1	1		
8 ns	0	0	1	0	0	0		
9 ns	0	0	1	0	0	1		
10 s	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61 ns	1	1	1	1	0	1		
62 ns	1	1	1	1	1	0		
63 ns	1	1	1	1	1	1		

Byte 37, SDRAM Minimum t_{WTR} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0 ns	See Subfield A						0	0
+.25 ns							0	1
+.50 ns							1	0
+.75 ns							1	1

Byte 38: Internal read to precharge command delay (t_{RTP})

This byte describes internal read to precharge command delay (t_{RTP})

Byte 38 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1 ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001010 (10 ns)	00 +(0.0 ns)	= 10.0 ns
000111 (7 ns)	10 +(.50 ns)	= 7.5 ns

Byte 38, SDRAM Minimum t_{RTP} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1 ns	0	0	0	0	0	1		
2 ns	0	0	0	0	1	0		
3 ns	0	0	0	0	1	1		
4 ns	0	0	0	1	0	0		
5 ns	0	0	0	1	0	1		
6 ns	0	0	0	1	1	0		
7 ns	0	0	0	1	1	1		
8 ns	0	0	1	0	0	0		
9 ns	0	0	1	0	0	1		
10 ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61 ns	1	1	1	1	0	1		
62 ns	1	1	1	1	1	0		
63 ns	1	1	1	1	1	1		

Byte 38, SDRAM Minimum t_{RTP} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0 ns	See Subfield A						0	0
+.25 ns							0	1
+.50 ns							1	0
+.75 ns							1	1

Byte 39: Memory Analysis Probe Characteristics

This byte describes various functional and parametric characteristics of the memory analysis probe connected to this DIMM slot. These characteristics may be consulted by the BIOS to determine proper bus drive strength to account for additional bus loading of the probe. It also describes functional characteristics of the probe that may be used to configure the memory controller to drive proper diagnostic signals to the probe, such as via the TEST,NC pin.

Detailed Features: TBD

Byte 40: Extension of Byte 41 tRC and Byte 42 tRFC

This field describes the extension of Byte 41 tRC and Byte 42 tRFC.

For example:

if module tRFC is:	byte 40								byte 42							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
127.5ns	0	X	X	X	0	1	1	0	0	1	1	1	1	1	1	1
327.5ns	0	X	X	X	0	1	1	1	0	1	0	0	0	1	1	1
if module tRC is:	**byte 40**								**byte 41**							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
63.75ns	0	1	0	1	X	X	X	X	0	0	1	1	1	1	1	1
65ns	0	0	0	0	X	X	X	X	0	1	0	0	0	0	0	1

Byte 40: Subfield A, Extension of Byte 42 tRFC (Bits 0)									
Line #	Minimum Refresh to Acitve/Refresh Command Period MSB	Bit 7 TBD	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A	Undefined	0	See Subfield C			See Subfield B			0
1A	256ns+byte 42	0							1

Byte 40: Subfield B, Extension of Byte 42 tRFC (Bits 1-3)									
Line #	Minimum Refresh to Active/Refresh Command Period LSB	Bit 7 TBD	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B	+0ns+byte 42	0	See Subfield C			0	0	0	See Subfield A
1B	+.25ns+byte 42	0				0	0	1	
2B	+.33ns+byte 42	0				0	1	0	
3B	+.5ns+byte 42	0				0	1	1	
4B	+.66ns+byte 42	0				1	0	0	
5B	+.75ns+byte 42	0				1	0	1	
6B	RFU	0				1	1	0	
-	Undefined	0				1	1	1	

Byte 40: Subfield C, Extension of Byte 41 tRC (Bits 4-6)									
Line #	Minimum Active to Active/Refresh Command Period LSB	Bit 7 TBD	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C	+0ns+byte 41	0	0	0	0	See Subfield B			See Subfield A
1C	+.25ns+byte 41	0	0	0	1				
2C	+.33ns+byte 41	0	0	1	0				
3C	+.5ns+byte 41	0	0	1	1				
4C	+.66ns+byte 41	0	1	0	0				
5C	+.75ns+byte 41	0	1	0	1				
6C	RFU	0	1	1	0				
-	Undefined	0	1	1	1				

Byte 41: SDRAM Device Minimum Activate to Activate/Refresh Time (t_{RC})

This byte identifies the minimum activate to activate or refresh time with Byte 40 as extension.

For example:

if module tRC is:	byte 40								byte 41							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
63.75 ns	0	1	0	1	X	X	X	X	0	0	1	1	1	1	1	1
65 ns	0	0	0	0	X	X	X	X	0	1	0	0	0	0	0	1

Byte 41									
Minimum Active to Active or Auto Refresh Time (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
Undefined	1	1	1	1	1	1	1	1	FF

Byte 42: SDRAM Device Minimum Refresh to Activate/Refresh Command Period (t_{RFC})

This byte identifies the minimum Refresh to Activate/Refresh Command Period (tRFC) with Byte 40 as extension.

For example:

If the module's tRFC is:	then Byte 40 is:	and Byte 42 is:
75	0XXX 0000	0100 1011
105	0XXX 0000	0110 1001
127.5	0XXX 0110	0111 1111
195	0XXX 0000	1100 0011
327.5	0XXX 0111	0100 0111

Byte 42									
Minimum Refresh to Active/Refresh Command Period (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.		.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF

Byte 43: SDRAM Device Maximum Device Cycle Time (tCK max)

This byte identifies the maximum device cycle time at any $\overline{\text{CAS}}$ latency. Byte 43 is split into two nibbles: the higher order nibble (bits 4-7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of .1ns and is added to the value designated by the higher nibble. In addition, four lines of the lower order nibble are assigned to support +.25,+.33, +.66 and +.75.

For example:

If bits 7:4 are	and bits 3:0 are	then the total time is:
1000	0000	
(8ns)	+ (0ns)	= 8.0ns

Byte 43, SDRAM Maximum Cycle Time, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	**Cycle Time**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield Table B				0_
1A	1ns	0	0	0	1					1_
2A	2ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1					F_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 43, SDRAM Maximum Cycle Time Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	**Cycle Time**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0B	+0ns	See Subfield Table B				0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	+.25ns					1	0	1	0	_A
11B	+.33ns					1	0	1	1	_B
12B	+.66ns					1	1	0	0	_C
13B	+.75ns					1	1	0	1	_D
-	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 44: SDRAM Device DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)

This byte identifies the maximum skew between DQS and all DQ signals for each device, in hundredths of nanoseconds.

Maximum Device DQS-DQ Skew (1/100 ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
0.01	0	0	0	0	0	0	0	1	01
0.02	0	0	0	0	0	0	1	0	02
0.03	0	0	0	0	0	0	1	1	03
0.04	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.50	0	0	1	1	0	0	1	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.60	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
2.54	1	1	1	1	1	1	1	0	FE
2.55	1	1	1	1	1	1	1	1	FF

Byte 45: SDRAM Device Read Data Hold Skew Factor (tQHS)

This byte identifies the maximum skew tQHS in hundreads of nanosconds.

For example:

Read data Hold Skew Factor(tQHS)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
0.01	0	0	0	0	0	0	0	1	01
0.02	0	0	0	0	0	0	1	0	02
0.03	0	0	0	0	0	0	1	1	03
0.04	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.50	0	0	1	1	0	0	1	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.60	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
2.54	1	1	1	1	1	1	1	0	FE
2.55	1	1	1	1	1	1	1	1	FF

Byte 46: PLL Relock Time

This byte describes the relock time of PLLs on the clock inputs.

PLL Relock Time (μs)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF

Byte 47: Tcasemax

This byte is split into two nibbles. The higher order nibble (bits 4:7) describes the DRAM case temperature difference between maximum case temperature and the baseline maximum case temperature of 85 degree C. Unit for this field is 2 degree C. The DRAM maximum case temperature is 85 degree C plus the value in bits 4:7. If bits 4:7 is zero, the DRAM device only supports up to 85 degree C maximum case temperature and users must ensure the case temperature will not exceed 85 degree C in any operation. If bits 4:7 is non-zero, the maximum case temperature range is extended and users must look at byte 49 bit 1 for the proper operation at this extended case temperature.

Byte 47: Tcasemax, Subfield A: 2 Degree C (Bits 7:4)										
Line #	Tcasemax (Unit: 2 ^{0}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	0	0	0	0	0					0-
1A	2	0	0	0	1					1-
2A	4	0	0	1	0					2-
3A	6	0	0	1	1	See Subfield B				3-
4A	8	0	1	0	0					4-
5A	10	0	1	0	1					5-
6A	12	0	1	1	0					6-
7A	14	0	1	1	1					7-
8A	16	1	0	0	0					8-
9A	18	1	0	0	1					9-
10A	20	1	0	1	0	See Subfield B				A-
.	.	.	.	.	.					.
.	.	.	.	.	.					.
14A	28	1	1	1	0					E-
15A	Exceed 30	1	1	1	1					F-

The lower order nibble (bits 0:3) describe DT4R4W Delta (the DRAM case temperature rise difference from ambient due to IDD4R/page open burst read vs. IDD4W/page open burst write operations) at VDD = 1.9 volt, in unit of 0.4 degree C. Please refer to JEDEC DDR2 DRAM Component Specification for the definitions of IDD4R and IDD4W operations. Please refer to Notes 6 & 7 of the"1.1 Address Map table" of this spec for calculation of temperature rise.

Byte 47: DT4R4W Delta, Subfield B: 0.4 Degree C (Bits 0:3)										
Line #	DT4R4W Delta (**Granularity**: 0.4 ^{0}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Not Supported					0	0	0	0	-0
1A	0.4					0	0	0	1	-1
2A	0.8					0	0	1	0	-2
3A	1.2					0	0	1	1	-3
4A	1.6					0	1	0	0	-4
5A	2.0					0	1	0	1	-5
6A	2.4					0	1	1	0	-6
7A	2.8					0	1	1	1	-7
8A	3.2	See Subfield A				1	0	0	0	-8
9A	3.6					1	0	0	1	-9
10A	4.0					1	0	1	0	-A
.	.					.	.	.	.	.
.	.					.	.	.	.	.
14A	5.6					1	1	1	0	-E
15A	Exceed 6.0					1	1	1	1	-F

Byte 48: Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi $_{T\text{-}A\ DRAM}$)

This byte describes the thermal resistance of DRAM package from top (case) to ambient and it is based on JESD51-3 “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages” under JESD51-2 standard. Unit for this field is 0.5 ^{O}C/W.

Byte 48: Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi $_{T\text{-}A\ DRAM}$)									
Psi T-A DRAM (**Granularity**: 0.5 ^{0}C/W)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Defined	0	0	0	0	0	0	0	0	00
0.5	0	0	0	0	0	0	0	1	01
1.0	0	0	0	0	0	0	1	0	02
1.5	0	0	0	0	0	0	1	1	03
2.0	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
16.0	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
30.0	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1	0	FE
Exceed 127.5	1	1	1	1	1	1	1	1	FF

Byte 49: DRAM Case Temperature Rise from Ambient due to Activate-Precharge/ Mode Bits (DT0/Mode Bits)

This byte is split into two fields. Bits 2:7 describe DT0 (DRAM case temperature rise from ambient due to IDD0/activate-precharge operation minus 2.8 degree C offset temperature), in unit of 0.3 degree C. The value in Bits 2:7 plus 2.8 degree C is the DRAM case temperature rise from ambient. Please refer to JEDEC DDR2 DRAM Component Specification for the definition of IDD0 operation. Please refer to Notes 6 & 7 of the "1.1 Address Map table" of this spec for calculation of temperature rise.

Byte 49: DT0, Subfield A: 0.3 Degree C (Bits 2:7)									
Line #	**DT0 (Granularity: 0.3^{0}C)**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0A	Not Defined	0	0	0	0	0	0		
1A	0.3	0	0	0	0	0	1		
2A	0.6	0	0	0	0	1	0		
3A	0.9	0	0	0	0	1	1		
4A	1.2	0	0	0	1	0	0		
5A	1.5	0	0	0	1	0	1	See Sub-field B	
6A	1.8	0	0	0	1	1	0		
7A	2.1	0	0	0	1	1	1		
8A	2.4	0	0	1	0	0	0		See subfield A
9A	2.7	0	0	1	0	0	1		
10A	3.0	0	0	1	0	1	0		
.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.		
62A	18.6	1	1	1	1	1	0		
63A	Exceed 18.9	1	1	1	1	1	1		

Bit 1 definition whether or not double refresh is required for DRAM case temperature exceeding 85 degree C.

Bit 1	Byte 49: Subfield B (Bit 1)
0	Do not need double refresh rate for the proper operation at the DRAM maximum case temperature above 85 degree C. The DRAM maximum case temperature is specified at Byte 47.
1	Requires double refresh rate for the proper operation at the DRAM maximum case temperature above 85 degree C. The DRAM maximum case temperature is specified at Byte 47.

Bit 0 indicates DDR2 SDRAM "High Temperature Self Refresh" support.

Bit 0	Byte 49: Subfield A (Bit 0)
0	DRAM does not support high temperature self-refresh entry. Controller must ensure DRAM cool down to Tcase < 85 degree C before entering self-refresh
1	DRAM high temperature self-refresh entry supported. When needed, controller may set DRAM in high temperature self-refresh mode via EMRS(2) [A7] and be able to enter self-refresh above 85 degree C Tcase temperature

Byte 50: DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)

For Unbuffered DIMM, this describes the DRAM case temperature rise from ambient due to IDD2N/precharge standby operation (DT2N) at VDD = 1.9 volt, in unit of 0.1 degree C. Please refer to JEDEC DDR2 DRAM Component Specification for the definition of IDD2N operation. Please refer to Notes 6 & 7 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

For Registered DIMM, this byte describes the DRAM case temperature rise from ambient due to IDD2Q/precharge quiet standby operation (DT2Q) at VDD = 1.9 volt, in unit of 0.1 degree C. Please refer to JEDEC DDR2 DRAM Component Specification for the definition of IDD2Q operation. Please refer to Notes 6 & 7 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT2N/2Q (Granularity: 0.1 ^{o}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.1	0	0	0	0	0	0	0	1	01
0.2	0	0	0	0	0	0	1	0	02
0.3	0	0	0	0	0	0	1	1	03
0.4	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
3.2	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
6.0	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25.4	1	1	1	1	1	1	1	0	FE
Exceed 25.5	1	1	1	1	1	1	1	1	FF

Byte 51: DRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P)

This byte describes the DRAM case temperature rise from ambient due to IDD2P/precharge power-down operation at VDD = 1.9 volt, in unit of 0.015 degree C. Please refer to JEDEC DDR2 DRAM Component Specification for IDD2P operation. Please refer to Notes 6 & 7 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT2P (Granularity: 0.015 ^{o}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.015	0	0	0	0	0	0	0	1	01
0.030	0	0	0	0	0	0	1	0	02
0.045	0	0	0	0	0	0	1	1	03
0.060	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.480	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.900	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
3.810	1	1	1	1	1	1	1	0	FE
Exceed 3.825	1	1	1	1	1	1	1	1	FF

Byte 52: DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)

This byte describes the DRAM case temperature rise from ambient due to IDD3N/active standby operation at VDD = 1.9 volt, in unit of 0.15 degree C. Please refer to JEDEC DDR2 DRAM Component Specification for IDD3N operation. Please refer to Notes 6 & 7 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT3N (Granularity: 0.15 ^{o}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.15	0	0	0	0	0	0	0	1	01
0.30	0	0	0	0	0	0	1	0	02
0.45	0	0	0	0	0	0	1	1	03
0.60	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
4.80	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
9.00	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
38.10	1	1	1	1	1	1	1	0	FE
Exceed 38.25	1	1	1	1	1	1	1	1	FF

Byte 53: DRAM Case temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)

This byte describes the DRAM case temperature rise from ambient due to IDD3P Fast PDN Exit/active power-down with fast PDN exit operation at VDD = 1.9 volt, in unit of 0.05 degree C. Please refer to JEDEC DDR2 DRAM Component Specification for IDD3P Fast PDN Exit operation. Please refer to Notes 6 & 7 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT3Pfast (Granularity: 0.05 ^{o}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.05	0	0	0	0	0	0	0	1	01
0.10	0	0	0	0	0	0	1	0	02
0.15	0	0	0	0	0	0	1	1	03
0.20	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1.60	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
3.00	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
12.70	1	1	1	1	1	1	1	0	FE
Exceed 12.75	1	1	1	1	1	1	1	1	FF

Byte 54: DRAM Case temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)

This byte describes the DRAM case temperature rise from ambient due to IDD3P Slow PDN Exit/active power-down with slow PDN exit operation at VDD = 1.9 volt, in unit of 0.025 degree C. Please refer to JEDEC DDR2 DRAM Component Specification for IDD3P Slow PDN Exit operation. Please refer to Notes 6 & 7 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT3Pslow (Granularity: 0.025 ^{o}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.025	0	0	0	0	0	0	0	1	01
0.050	0	0	0	0	0	0	1	0	02
0.075	0	0	0	0	0	0	1	1	03
0.100	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.800	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1.500	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
6.350	1	1	1	1	1	1	1	0	FE
Exceed 6.375	1	1	1	1	1	1	1	1	FF

Byte 55: DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/ DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)

This byte is split into two fields: bits 1:7 describes the DRAM case temperature rise from ambient due to IDD4R/page open read operation at VDD = 1.9 volt, in unit of 0.4 degree C. Please refer to JEDEC DDR2 DRAM Component Specification for the definition of IDD4R operation. Please refer to Notes 6 & 7 of the "1.1 Address Map table" of this spec for calculation of temperature rise. Bit 0 specifies if DT4W (Case temperature rise from ambient due to page open burst write) is greater than or less than DT4R.

Byte 55: DT4R, Subfield A: 0.4 Degree C (Bits 1:7)									
Line #	**DT4R (Granularity: 0.4 ^{o}C)**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0A	Not Supported	0	0	0	0	0	0	0	
1A	0.4	0	0	0	0	0	0	1	
2A	0.8	0	0	0	0	0	1	0	
3A	1.2	0	0	0	0	0	1	1	
4A	1.6	0	0	0	0	1	0	0	
5A	2.0	0	0	0	0	1	0	1	See Sub-field B
6A	2.4	0	0	0	0	1	1	1	
7A	2.8	0	0	0	1	0	0	0	
8A	3.2	0	0	0	1	0	0	1	
9A	3.6	0	0	0	1	0	1	0	
10A	4.0	0	0	0	1	0	1	1	
.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	
126A	50.4	1	1	1	1	1	1	0	
127A	Exceed 50.8	1	1	1	1	1	1	1	

Byte 55: DT4R4W Mode Bit, Subfield B: 0.4 Degree C (Bit 0)									
Line #	**DT4R4W Mode Bit**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0A	DT4W is greater than DT4R			See Subfield A					0
1A	DT4W is less than DT4R								1

Byte 56: DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)

This byte describes the DRAM case temperature rise from ambient due to IDD5B/burst refresh operation at VDD = 1.9 volt, in unit of 0.5 degree C. Please refer to JEDEC DDR2 DRAM Component Specification for the definition of IDD5B operation. Please refer to Notes 6 & 7 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT5B (Granularity: 0.5 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.5	0	0	0	0	0	0	0	1	01
1.0	0	0	0	0	0	0	1	0	02
1.5	0	0	0	0	0	0	1	1	03
2.0	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
16.0	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
30.0	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127.0	1	1	1	1	1	1	1	0	FE
Exceed 127.5	1	1	1	1	1	1	1	1	FF

Byte 57: DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)

This byte describes the DRAM case temperature rise from ambient due to IDD7/bank interleave read with auto-precharge operation at VDD = 1.9 volt, in unit of 0.5 degree C. Please refer to Notes 6 & 7 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT7 (Granularity: 0.5 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.5	0	0	0	0	0	0	0	1	01
1.0	0	0	0	0	0	0	1	0	02
1.5	0	0	0	0	0	0	1	1	03
2.0	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
16.0	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
30.0	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127.0	1	1	1	1	1	1	1	0	FE
Exceed 127.5	1	1	1	1	1	1	1	1	FF

Byte 58: Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi $_{T\text{-}A\ PLL}$)

This byte describes the thermal resistance of PLL package from top (case) to ambient and it is based on JESD51-3 “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages” under JESD51-2 standard. Unit for this byte is 0.5 degree C/W.

Byte 58: Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi $_{T\text{-}A\ PLL}$)									
Psi T-A PLL(Granularity: 0.5 ^{0}C/W)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.5	0	0	0	0	0	0	0	1	01
1.0	0	0	0	0	0	0	1	0	02
1.5	0	0	0	0	0	0	1	1	03
2.0	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
16.0	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
30.0	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1	0	FE
Exceed 127.5	1	1	1	1	1	1	1	1	FF

Byte 59: Thermal Resistance of Register Package from Top (Case) to Ambient (Psi $_{T\text{-}A\ Register}$)

This byte describes the thermal resistance of register package from top (case) to ambient and it is based on JESD51-3 “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages” under JESD51-2 standard. Unit for this byte is 0.5 degree C/W.

Byte 59: Thermal Resistance of Register Package from Top (Case) to Ambient (Psi $_{T\text{-}A\ Register}$)									
Psi T-A Register (Granularity: 0.5 ^{0}C/W)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.5	0	0	0	0	0	0	0	1	01
1.0	0	0	0	0	0	0	1	0	02
1.5	0	0	0	0	0	0	1	1	03
2.0	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
16.0	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
30.0	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1	0	FE
Exceed 127.5	1	1	1	1	1	1	1	1	FF

Byte 60: PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)

This byte describes the PLL case temperature rise from ambient due to PLL in active mode with clock running within spec and OE enabled and at VDD = 1.9 volt, in unit of 0.25 degree C. The PLL loading is the DIMM loading. Registers being used in the DIMM may have different variants, like single rank, dual ranks, dual ranks without parity. This SPD field needs to correspond to the respective DIMM configuration. Please refer to Byte 21 to determine the number of PLLs on the DIMM. Please refer to Notes 9 & 11 of the "1.1 Address Map table" of this spec for calculation of temperature rise.

DT PLL Active (Granularity: 0.25 ^{o}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.25	0	0	0	0	0	0	0	1	01
0.50	0	0	0	0	0	0	1	0	02
0.75	0	0	0	0	0	0	1	1	03
1.00	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
8.00	0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
15.00	0	0	1	1	1	1	0	0	3C
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
63.50	1	1	1	1	1	1	1	0	FE
Exceed 63.75	1	1	1	1	1	1	1	1	FF

Byte 61: Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)

This byte is split into two fields. Bits 2:7 describes the register case temperature rise from ambient due to register in active mode with clock running within spec and OE enabled and at VDD = 1.9 volt. The register loading is the registered DIMM loading. Registers being used in registered DIMM may have different variants, like single rank, dual ranks, dual ranks without parity. This SPD field needs to correspond to the respective Registered DIMM configuration. Please refer to Notes 9 & 11 of the "1.1 Address Map table" of this spec for calculation of temperature rise. If there are multiple register components on the registered DIMM, this byte is still calculated using the IDD value of one of the registers. Please refer to Byte 21 to determine the number of registers on the DIMM. Bit 1 is reserved for future use (RFU). Default value is 0. Bit 0 specifies the register data output toggle rate and it shall be consistent with the maximum data toggle rate specified in the IDD specification in the JEDEC DDR2 DRAM Component Specification.

Byte 61: DT Register Active, Subfield A: (Bit 0)									
Line #	DT Register Active Mode Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A	50% register data output toggle			See Subfield B				RFU. Default: 0	0
1A	100% register data output toggle								1

If Bit 0	Unit for Bits 2:7 (^{o}C)
0	0.75
1	1.25

Byte 61: DT Register Active, Subfield B: 0.75 Degree C (Bits 2:7) if Bit 0 = 0									
Line #	DT Register Active (**Granularity**: 0.75^{o}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A	Not Supported	0	0	0	0	0	0		
1A	0.75	0	0	0	0	0	1		
2A	1.50	0	0	0	0	1	0	RFU. Default: 0	Value = 0. See Subfield A
3A	2.25	0	0	0	0	1	1		
4A	3.00	0	0	0	1	0	0		
5A	3.75	0	0	0	1	0	1		
6A	4.50	0	0	0	1	1	0		
7A	5.25	0	0	0	1	1	1		
8A	6.00	0	0	1	0	0	0		
9A	6.75	0	0	1	0	0	1		
10A	7.50	0	0	1	0	1	0		
.	.	.	.	.	.	.	.		
62A	46.50	1	1	1	1	1	0		
63A	Exceed 47.25	1	1	1	1	1	1		

Byte 61: DT Register Active, Subfield B: 1.25 Degree C (Bits 2:7) if Bit 0 = 1									
Line #	DT Register Active (**Granularity**: 1.25^{o}C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A	Not Supported	0	0	0	0	0	0		
1A	1.25	0	0	0	0	0	1		
2A	2.50	0	0	0	0	1	0		
3A	3.75	0	0	0	0	1	1		
4A	5.00	0	0	0	1	0	0		
5A	6.25	0	0	0	1	0	1	RFU. Default: 0	Value = 1. See Subfield A
6A	7.50	0	0	0	1	1	0		
7A	8.75	0	0	0	1	1	1		
8A	10.00	0	0	1	0	0	0		
9A	11.25	0	0	1	0	0	1		
10A	12.50	0	0	1	0	1	0		
.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.		
62A	77.5	1	1	1	1	1	0		
63A	Exceed 78.75	1	1	1	1	1	1		

An Illustration Example of DT in SPD

This section shows an example of programming SPD Byte 21 bit 3:0 and Byte 47 ~ 61. All the numbers in the tables below are arbitrary and for the sole purpose of demonstrating how to program SPD Byte 21 bit 3:0 and Byte 47 ~ 61. They are NOT intended to reflect any actual device properties.

DT in SPD											Example For Reference Only			
BYTE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex		Parameter Description	Parameter Value	Byte Value	Byte Unit
21	-	-	-	-	0	1	0	0	-4		Number of PLLs/active registers on the DIMM	1 / 1	-4	1 PLL / 1 active register
47	0	0	0	0	0	0	1	0	02		Tcasemax / DT4R4W Delta = DT (7mA)	85 ^{o}C/0.84^{o}C	0 / 2	0.4 ^{o}C
48	0	1	1	1	1	1	1	0	7E		Psi T-A DRAM	63.2 ^{o}C/W	126	0.5 ^{o}C/W
49	0	1	0	0	0	1	0	-	Bit 7:1: 22		DT0 = DT (65mA) /Tcase Mode Bits	4.98^{o}C / Do not need double refresh.	Bit 7:2 / Bit 1: 17 / 0	0.3 ^{o}C
50 (UDIMM)	0	0	1	0	0	0	1	0	22		DT2N = DT (28mA)	3.35 ^{o}C	34	0.1 ^{o}C
50 (RDIMM)	0	0	0	1	0	1	1	1	17		DT2Q = DT (19mA)	2.27 ^{o}C	23	0.1 ^{o}C
51	0	0	0	1	1	0	0	0	18		DT2P = DT (3mA)	0.36 ^{o}C	24	0.015^{o}C
52	0	0	0	1	1	0	0	1	19		DT3N = DT (31mA)	3.71 ^{o}C	25	0.15 ^{o}C
53	0	0	0	1	1	0	1	0	1A		DT3P fast = DT (11mA)	1.32 ^{o}C	26	0.05 ^{o}C
54	0	0	0	1	1	0	0	0	18		DT3P slow = DT (5mA)	0.60 ^{o}C	24	0.025 ^{o}C
55	0	0	1	0	1	0	1	0	2A		DT4R = DT(70mA) / DT4R4W Mode bit	8.38^{o}C/0	21	0.4 ^{o}C
56	0	0	0	1	1	1	1	1	1F		DT5B = DT (128mA)	15.32 ^{o}C	31	0.5 ^{o}C
57	0	0	1	0	1	0	0	0	28		DT7 = DT (165mA)	19.8 ^{o}C	40	0.5 ^{o}C
58	1	0	1	1	0	1	0	0	B4		Psi T-A PLL	90 ^{o}C/W	180	0.5 ^{o}C/W
59	1	0	1	0	0	0	0	0	A0		Psi T-A Register	80 ^{o}C/W	160	0.5 ^{o}C/W
60	0	1	0	0	0	1	0	0	44		DT PLL Active = DT (100mA)	17.1 ^{o}C	68	0.25 ^{o}C
61	0	1	1	1	1	0	RFU (0)	0	78		DT Register Active = DT (150mA)	22.8 ^{o}C/0	30	0.75 ^{o}C

In the example listed in the table above, Psi T-A DRAM true value is 63.2 ^{o}C/W and unit is 0.5 ^{o}C/W, Byte value is determined as following: 63.2 / 0.5 = 126.4. Since 126.4 is closer to 126 then it is to 127, therefore the programmed SPD Byte value is rounded off to 126.

Also in the example listed in the table above, SPD Byte value for DT3P fast is calculated as following:

DT3P fast= IDD3P fast* 1.9 Volt * Programmed value of Psi T-A DRAM

= 11mA * 1.9 volt * (Value in Byte 48 * Byte 48 Unit)

= 11mA * 1.9 volt * (126 * 0.5 C/W)

= 1.32 ^{o}C

DT3P fast SPD byte unit is 0.05 ^{o}C, 1.32 ^{o}C/ 0.05 ^{o}C = 26.4. Since 26.4 is closer to 26 than it is to 27, therefore the programmed value for SPD byte 53 (DT3P fast) is rounded off to 26 (Hex value 1A).

Byte 62: SPD Revision

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. This byte must be coded as 10h for SPDs with revision level 1.0. Software should examine the upper nibble(Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 00h or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

SPD Revision	Encoding Level				Additions Level				Hex
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Revision 0.0	0	0	0	0	0	0	0	0	00
Undefined	0	0	0	0	0	0	0	1	01
...	.	.	.	.	.	.	.	.	.
Revision 1.0	0	0	0	1	0	0	0	0	10
Revision 1.1	0	0	0	1	0	0	0	1	11
...	.	.	.	.	.	.	.	.	...
Undefined	1	1	1	1	1	1	1	1	FF

Byte 63: Checksum for Bytes 0-62

This field designates the checksum for checking data integrity (similar to parity) for bytes 0 - 62. It is written during module production and can be used by the customer to verify the data integrity for these bytes.

Process for Calculating the Checksum

1. Convert binary information, in byte locations 0 - 62, to decimal.
2. Add together (sum) all decimal values for addresses 0 - 62.
3. Divide sum by 256.
4. Convert remainder to binary (will be less than 256).
5. Store result (single byte) in address 63 as “Checksum.”

Note: The same result can be obtained by adding the binary values in addresses 0 - 62 and eliminating all but the low order byte. The low order byte is the “Checksum.”

Example of a Checksum Calculation

SPD Byte Address	Serial PD		Convert to Decimal
0	0010 0100	→	36
1	1111 1110	→	+254
2	0000 0000	→	+ 0
3	0000 0000	→	+ 0
↓	↓	→	+ 0
		→	+ 0
60	0000 0000	→	+ 0
61	0000 0000	→	+ 0
62	0000 0000	→	+ 0
Decimal Total	-	-	290
Divide by 256	-	-	1
Remainder	-	-	34
Convert to binary	0010 0010	←	34
63 (Checksum)	0010 0010	-	-

Bytes 64-71: Module Manufacturer’s JEDEC ID Code

Manufacturers of a given module may include their identifier according to JEDEC spec JEP106. The first byte is utilized, the second byte is filled with zeros. For example, a company whose value is hexadecimal CE would be coded as: “CE000000 00000000.”

Byte 72: Module Manufacturing Location

Manufacturers may include an identifier that uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

Bytes 73-90: Module Part Number

The manufacturer's part number is written in ASCII format within these bytes. Unused digits are coded as ASCII blanks (20h).

Bytes 91-92: Module Revision Code

This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

Bytes 93-94: Module Manufacturing Date

The module manufacturer includes a date code for the module. The JEDEC definitions for bytes 93 and 94 are year and week respectively. These bytes must be represented in Binary Coded Decimal (BCD). For example, week 47 in year 2003 would be coded as 03 (0000 0011) in byte 93 and 47 (0100 0111) in byte 94.

Bytes 95-98: Module Serial Number

The supplier must include a unique serial number for the module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

One method of achieving this is by assigning a byte in the field from 95-98 as a tester ID byte and using the remaining bytes as a sequential serial number. Using bytes 64-72 and 93-98 to construct a unique serial number results in a field that contains 15 bytes of data. A shortened unique serial number containing 9 bytes of data can be derived from the SPD bytes by reducing the manufacturers ID in bytes 64-71 to 2 bytes, where the first byte indicates the quantity of 0x7F "continuation characters" in bytes 64-71, and the second byte is the 1-byte manufacturers ID following the last 0x7F "continuation character" (ref: JEDEC JEP106N), Any characters following the 1-byte manufacturers ID are ingored for the purposes of constructing the value of the shortened unique serial number.

Bytes 99-127: Manufacturer's Specific Data

The module manufacturer may include any additional information desired into the module within these locations.

Bytes 128-255: Open for Customer Use

These bytes are unused by the manufacturer and are open for customer use.

Appendix: ASCII Decode Matrix for SPDs

The following table is a subset of the full ASCII standard which is used for coding bytes in the Serial Presence Detect EEPROM that require ASCII characters:

	Second Hex Digit in Pair															
First Hex Digit in Pair	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	Blank Space								(	)				- Dash	.	
3	0	1	2	3	4	5	6	7	8	9						
4		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z					
6		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z					

Examples:

20h=Blank Space
34h=4
41h=A

SPD Bytes 73-90	
Manufacturer's PN	Coded in ASCII
13M32734BCD-260Y	31334D3332373334424344 2D323630592020

Revision Log

Rev	Contents of Modification
Feb. 2003	First release - BoD approved DDR2 SPD revision 1.0
Jan. 2004	DDR2 SPD revision 1.1 1. Changed " Wording of Byte 93 and 94" - rb03170 passed committee ballot at Sep. 03 meeting 2. Added Command and Address Parity feature to Byte 11 - rb03230 passed committee ballot at Dec. 03 meeting 3. Added number of PLL and register feature on Byte 21 bits [3:0] - rb03246 passed committee ballot at Dec. 03 meeting 4. Added Byte 47 ~ 61, DT in SPD - rb03246 passed committee ballot at Dec. 03 meeting 5. Added "Self refresh period at high temp" feature to Byte 49 - rb03247 passed committee ballot at Dec. 03 meeting 6. Corrected typos